In the Claims:

1. (Currently Amended) A semiconductor device for storing electrons representing dual data bits with improved write/erase characteristics comprising:

a substrate defining at least one channel region having a selected width and separating areas of buried diffusion;

a bottom dielectric formed over said channel region and having a first edge and a second edge;

a data storage layer formed over said bottom dielectric, said data storage layer comprising a middle dielectric extending between first and second end surfaces, and covering an intermediate portion of said bottom dielectric, said middle dielectric collecting and storing said electrons therein adjacent said first and second end surfaces as said dual data bits, a first floating gate extending over said bottom dielectric from said first edge to said first end surface of said middle dielectric and a second floating gate extending over said bottom dielectric from said second edge to said middle dielectric;

a top dielectric covering said data storage layer; and

a gate electrode formed over said top dielectric.

2. (Original) The semiconductor device of claim 1 further comprising spacers formed at the edges of said bottom dielectric, said data storage layer, said top dielectric and said gate electrode.

3. (Original) The semiconductor device of claim 1 wherein said bottom dielectric is silicon oxide.

4. (Original) The semiconductor device of claim 3 wherein said top dielectric is silicon oxide.

5. (Original) The semiconductor device of claim 3 wherein said middle dielectric is silicon nitride.

6. (Original) The semiconductor device of claim 4 wherein said middle dielectric is silicon nitride.

7. (Original) The semiconductor device of claim 3 wherein said bottom dielectric has a thickness of between about 70 and about 100 Å.

8. (Original) The semiconductor device claim 4 wherein said top dielectric has a thickness of between about 70 and about 100 Å

9. (Original) The semiconductor device of claim 5 wherein said middle dielectric has thickness of between about 50 and about 70 Å.

10. (Original) The semiconductor device of claim 1 wherein said gate electrode is a layer of poly silicon.

11. (Original) The semiconductor device of claim 1 wherein said first floating gate is made of poly silicon.

12. (Original) The semiconductor device of claim 1 wherein said second floating gate is made of poly silicon.

13. (Original) The semiconductor device of claim 1 wherein said first and second floating gates are made of poly silicon.

14. (Currently Amended) An ONO semiconductor device for storing electrons representing dual data bits with improved write/erase characteristics comprising:

a substrate defining at least one channel region having a selected width and separating areas of buried diffusion;

a first oxide dielectric formed over said channel region and having a first edge and a second edge;

a data storage layer formed over said first oxide dielectric layer, said data storage layer comprising a nitride dielectric layer extending between first an second end surfaces and covering an intermediate portion of said first oxide dielectric layer, said nitride dielectric layer collecting and storing said electrons therein adjacent to said first and second end surfaces as said dual data bits, a first poly silicon floating gate extending over said oxide dielectric layer from said first edge to said first end surface of said nitride dielectric and a second poly silicon floating gate extending over said oxide dielectric layer from said second edge to said second end surface of said nitride dielectric;

a second oxide dielectric layer covering said data storage layer; and

a poly silicon layer formed over said second oxide dielectric layer.

15. (Original) The semiconductor device of claim 14 further comprising spacers formed at the edges of said first oxide layer, said data storage layer, said second oxide dielectric layer and said poly silicon layer.

16. (Original) The semiconductor device of claim 14 wherein said first oxide layer is silicon oxide.

17. (Original) The semiconductor device of claim 16 wherein said second oxide layer is silicon oxide.

18. (Currently Amended) The semiconductor device of claim 16 wherein said nitride dielectric layer is silicon nitride.

19. (Original) The semiconductor device of claim 17 wherein said nitride dielectric layer is silicon nitride.

20. (Original) The semiconductor device of claim 16 wherein said first oxide layer has a thickness of between about 70 and about 100 Å.

21. (Original) The semiconductor device of claim 17 wherein said second oxide layer has a thickness of between about 70 and about100 Å.

22. (Original) The semiconductor device of claim 18 wherein said nitride dielectric layer has thickness of between about 50 and about 70 Å.

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49. (New) The semiconductor device of claim 1 further comprising an oxide portion formed on said first and second end surfaces.

50. (New) The ONO semiconductor device of claim 14 further comprising an oxide portion formed on said first and second end surfaces.